

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

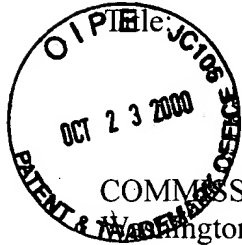
Applicant(s): David L. Reese, et al.

Serial No.: 09/322,443

Art Unit: 2751

Filed: May 28, 1999

Examiner: unassigned

PROFILING OF COMPUTER PROGRAMS EXECUTING IN VIRTUAL
MEMORY SYSTEMS

INFORMATION DISCLOSURE STATEMENT

COMMISSIONER FOR PATENTS

Washington, D.C. 20231

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In accordance with 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant wishes to make of record the enclosed items, as listed on the accompanying Form PTO-1449. Applicant respectfully requests the Examiner to fully consider the items and independently ascertain their teaching before issuance of the next action, and to make them of record in the file. The Examiner is also requested to initial and return a copy of the enclosed Form PTO-1449 to evidence such consideration.

The Form 1449 filed herewith is cumulative of several previously-filed forms 1449. The Examiner may disregard the earlier 1449's. It is hoped that having all references listed on one 1449 will be a convenience for the Examiner. If it in fact raises an inconvenience, Applicant apologizes for lack of knowledge of Office procedure.

Of the references listed on the enclosed Form 1449, the following are believed to be the most pertinent:

- Anton Chernoff, et al., FX!32, A Profile-Directed Binary Translator
- T.M. Conte, et al., "Hardware based profiling: An effective technique for profile-driven optimization,"
- J.S. Cox et al., "Commercializing profile-driven optimization."
- Ebcioglu and Altman, IBM Research Report, DAISY: Dynamic Compilation for 100% Architectural Compatibility.

The most pertinent portion of the Baxter '602 patent is believed to be Fig. 103, Fig. 110, col. 212, and cols. 345-358, though even that portion of Baxter '602 is only slightly pertinent. The Examiner is requested to independently ascertain the teaching and evaluate the relevance of each item cited on the Form 1449.

I certify that this correspondence, along with any documents referred to therein, is being deposited with the United States Postal Service on October 19, 2000 as First Class Mail in an envelope with sufficient postage addressed to The Commissioner for Patents, Washington D.C. 20231.

For any item listed on the enclosed copy of Form PTO-1449 for which a copy is not already made of record in this application, a copy was previously cited by or submitted to the Patent and Trademark Office in application Serial No. 09/239,194, filed January 28, 1999, Yates et al., Executing Programs for a First Computer Architecture on a Computer of a Second Architecture.

This application is one of a group of applications having similar disclosures. The Examiner is requested to be aware of these other applications, both with respect to potential double patenting issues and with respect to prior art that may be discovered in other applications.

Serial No.	Filing Date	Title
✓ 09/239,194	1/28/1999	Executing Programs for a First Computer Architecture on a Computer of a Second Architecture
✓ 09/330,852	6/11/1999	Profiling Ranges of Execution of a Computer Program
✓ 09/332,263	6/11/1999	Profiling Program Execution By Dense Trace Profiling and Statistical Profiling
✓ 09/334,530	6/16/1999	Profiling Execution of Computer Programs
✓ 09/339,749	6/24/1999	Profiling Program Execution into Registers of a Computer
✓ 09/339,797	6/24/1999	Modifying Program Execution Based on Profiling
✓ 09/348,317	7/7/1999	Recording Classification of Instructions Executed by a Computer
✓ 09/385,394	8/30/1999	Computer For Executing Two Different Instruction Sets
✓ 09/425,401	10/22/1999	Profiling Program Execution to Identify Frequently Executed Portions and to Assist Binary Translation
✓ 09/426,989	10/26/1999	Table Look-up For Control of Instruction Execution
✓ 09/427,168	10/26/1999	Transferring Execution From One Computer Instruction Stream to Another
09/428,850	10/28/1999	Recording I/O Memory References in Program Execution Profile
09/429,094	10/28/1999	Side Tables Annotating an Instruction Stream
09/429,377	10/28/1999	Improving Computer Execution by Opportunistic Adaptation
09/432,752	11/3/1999	Detecting Invalidation of Translated Object Code when Source Object Code is Modified (XP bit)
09/432,753	11/3/1999	Safety-Net Paradigm for Managing Two Execution Modes
09/434,198	11/4/1999	Detecting Modification to Computer Memory by a DMA Device
09/434,394	11/4/1999	Detecting Reordered Side-Effects
09/626,325	7/26/2000	Computer with Two Operating Systems
09/666,110	9/20/2000	Computer for Execution of Two Instruction Sets
09/667,226	9/21/2000	Exception Mechanism for a Computer
09/672,424	9/28/2000	Complex Instruction Set Computer
09/672,440	9/28/2000	Managing Instruction Side-Effects
09/672,841	9/28/2000	Validation of Memory References

A number of references are being made of record in these other applications in Information Disclosure Statements being filed contemporaneously herewith. It is believed that none of the references made of record in these other applications are pertinent to the claims of the current application, except those that are made of record in this application and listed in this Form 1449. Nonetheless, the Examiner is requested to be aware of these additional items.

Recent commercial efforts in the general field have included the FX!32 project of Digital Equipment Corporation, the Crusoe project of Transmeta Corp., the Merced/Itanium project at Intel and Hewlett-Packard, and projects at NexGen and Exponential Technology, Inc.

The VAX 11/780 computer, introduced by Digital Equipment Corp. in the late 1970's, had some capability to execute programs for a first computer architecture on a computer of a second architecture.

Since the early 1960's, IBM has offered emulation and simulation modes whereby its computers could execute program binaries for earlier IBM processors.

It is not believed that the capabilities of any of these prior computers relate to the inventions claimed in this application; nonetheless, the examiner's attention is drawn to these machines as possibly relevant prior art.

No fee is due under 37 C.F.R. §1.17(p) for this Information Disclosure Statement since it is being filed in compliance with 37 C.F.R. §1.97(b)(3), to the knowledge of the undersigned, before the mailing date of a first Office Action on the merits.

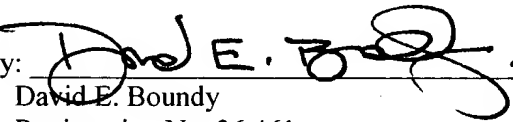
The Commissioner is hereby authorized to charge any additional fees that may be required for this Information Disclosure Statement, or credit any overpayment, to Deposit Account 50-0324, Order No. 30585/6.

Respectfully submitted,

SHEARMAN & STERLING

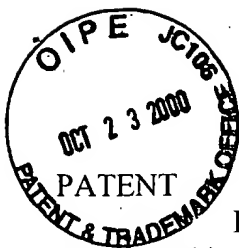
Dated: October 19, 2000

By:


David E. Boundy
Registration No. 36,461

CORRESPONDENCE ADDRESS:

SHEARMAN & STERLING
599 Lexington Avenue
New York, New York 10022
(212) 848-4000
(212) 848-7179 Facsimile



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DOCKET NO. 30585/6

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CERTIFICATE OF MAILING (37 C.F.R. 1.8a)

COMMISSIONER FOR PATENTS

Washington, D.C. 20231

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I hereby certify that the attached

1. Return postcard
2. This Certificate of Mailing
3. Information Disclosure Statement and Form PTO-1449
4. two references

along with any paper(s) referred to as being attached or enclosed) and this Certificate of Mailing are being deposited with the United States Postal Service on date shown below with sufficient postage as first-class mail in an envelope addressed to the: Commissioner for Patents, Washington, D.C. 20231.

Respectfully submitted,

SHEARMAN & STERLING

Dated: October 19, 2000

By: David E. Boundy

David E. Boundy
Registration No. 36,461

Mailing Address:

SHEARMAN & STERLING
599 Lexington Avenue
New York, New York 10022
(212) 848-4000
(212) 848-7179 Telecopier